IN THE CLAIMS

Please amend the pending claims as follows:

1. (currently amended) A method for controlling the access to all or part of the content of a first memory [[(2, 3)]] integrated with a microprocessor ~~(10), consisting of~~ comprising:

using a priority-holding interrupt (PRIORIN);

using at least one register of keys [[(21)]]; and

applying at least one access control algorithm contained in a second auxiliary memory [[(20)]] distinct from the first memory and using the content of at least one also integrated storage element [[(2)]] and the content of the key register, the content of the auxiliary memory being programmable only once.

2. (currently amended) The method of claim 1, wherein at least one sub-program authorizing the execution of a function of access to the first memory [[(2, 3)]] is contained in the auxiliary memory [[(20)]].

3. (original) The method of claim 1, wherein the priority-holding interrupt (PRIORIN) is non-interruptible, even by itself.

4. (original) The method of claim 1, wherein said priority-holding interrupt (PRIORIN) is generated provided that a signal (MODE) indicative of an access control operating mode is in an active state.

5. (original) The method of claim 1, wherein said priority-holding interrupt (PRIORIN) can be generated upon occurrence of an interrupt request coming from the outside (EXTPRIORIN) of the integrated circuit or from the inside (INTPRIORIN).

6. (currently amended) The method of claim 1, wherein said first memory is a program memory [[(2)]] containing embarked functions.

7. (currently amended) The method of claim 6, wherein said storage element is formed by the program memory [[(2)]].

8. (currently amended) A circuit integrating a microprocessor [[(10)]] and at least one first memory [[(2, 3)]], which includes a second auxiliary memory [[(20)]] adapted to containing at least one sub-program enabling authorizing the execution of a function of access to said first memory [[(2, 3)]], said auxiliary memory [[(20)]] distinct from the first memory and being programmable only once.

9. (currently amended) The circuit of claim 8, including means [[(22)]] for selecting, at the input of a memory interface [[(14)]] of the microprocessor [[(10)]], a memory from among at least:

said auxiliary memory [[(20)]]; and

said first memory [[(2, 3)]], the selection of said first memory, otherwise that for the execution of a function that it contains, requiring an authorization from an algorithm contained in the auxiliary memory and using the content of at least one also integrated storage element [[(2)]] and the content of the key register.

10. (currently amended) The circuit of claim 9, wherein the first memory and the storage element are one and the same program memory [[(2)]].

11. (currently amended) The circuit of claim 8, including means [[(24)]] for generating a priority-holding interrupt for executing said sub-program, the generation occurring provided that:

a signal (MODE) indicative of an access-control operating mode is in an active state;

an access to the first memory [[(2)]] has been requested otherwise than for a non-interruptible execution of one of the functions that it contains; and

an interrupt signal (EXTPRIORIN, INTPRIORIN) is active, the resulting priority-holding interrupt being non-interruptible, even by itself.

12. (original) The circuit of claim 8, including means for implementing the access control method of any of claims 1 to 7.